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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	RESPONSE UNDER 37 CFR 1.116
	:	EXPEDITED PROCEDURE
Evgueniy N. Stefanov et al.	:	EXAMINING GROUP 2815
	:	
Serial No.: 10/615,171	:	
Filed: July 9, 2003	:	Examiner: Matthew E. Warren

For: **SYMMETRICAL HIGH FREQUENCY SCR STRUCTURE**

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FAX No. (703) 872-9306 on March 2, 2005

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17 pages

AMENDMENT AFTER FINAL

Honorable Commissioner for Patents,
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

In response to the Office Action mailed December 30, 2004, please reconsider the above-identified patent application in view of the amendments and remarks presented hereinafter.

Amendments to the Claims

1. (previously presented): A high frequency integrated circuit structure comprising:

a body of semiconductor material having a plurality of isolated active regions, and comprising a first conductivity type;

internal circuitry formed in a first active region;

a second active region comprising a buried layer of a second conductivity type formed over the body of semiconductor material and a first semiconductor layer of the second conductivity type formed over the buried layer, wherein the first semiconductor layer has a lower dopant concentration than the buried layer;

a first silicon controlled rectifier device formed in the second active region, the first silicon controlled rectifier device comprising a first well region of the first conductivity type formed in the first semiconductor layer, a first doped region of the first conductivity type formed in the first well region, the buried layer, a second well region of the first conductivity type formed in the first semiconductor layer and spaced apart from the first well region, and a second doped region of the second conductivity type formed in the second well region; and

a second silicon controlled rectifier device comprising the second well region, a third doped region of the first conductivity type formed in the second well region, the buried layer, the first well region, and a fourth doped region of the second conductivity type formed in the first well region, wherein the first and second silicon controlled rectifier devices are coupled to the internal circuitry and form an ESD structure for protecting the internal circuitry against positive and negative ESD stresses.

2. (previously presented): The high frequency integrated circuit structure of claim 1 wherein the body of semiconductor material comprises:

a semiconductor wafer having the first conductivity type; and

a second semiconductor layer formed over the semiconductor wafer, wherein the second semiconductor layer comprises the first conductivity type, and wherein the second semiconductor layer has a lower dopant concentration than the semiconductor wafer, and wherein the buried layer is formed adjacent the second semiconductor layer.

3. (original): The high frequency integrated circuit device of claim 2 further comprising:

a first ohmic contact coupling the first and fourth doped regions; and

a second ohmic contact coupling the second and third doped regions.

4. (previously presented): The high frequency integrated circuit device of claim 2 further comprising a deep contact trench extending from a surface of the first semiconductor layer into the semiconductor wafer.

5. (previously presented): The high frequency integrated circuit device of claim 1 further comprising a field dielectric region formed on a surface of the first semiconductor layer between the first and second wells.

6. (currently amended): The high frequency integrated circuit structure of claim 2, wherein the second semiconductor layer has a dopant concentration of approximately 1.0×10^{13} atoms/cm^3.

7. (previously presented): the high frequency integrated circuit structure of claim 2, wherein the second semiconductor layer has a thickness from about 1.5 microns to about 3.0 microns.

8. (previously presented): The high frequency integrated circuit structure of claim 1 further comprising a deep isolation trench formed in the body of semiconductor material for isolating the ESD structure from the internal circuitry, wherein the deep isolation trench includes a dielectric layer.

9. (currently amended): A symmetrical SCR device comprising:

a semiconductor substrate of a first conductivity type;

a first semiconductor layer of the first conductivity type formed over the semiconductor substrate, wherein the first semiconductor layer has a lower dopant concentration than the semiconductor substrate;

a second semiconductor layer of a second conductivity type formed adjacent the first semiconductor layer;

a third semiconductor layer of the second conductivity type formed adjacent the second semiconductor layer, wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer;

first and second wells comprising the ~~second~~ first conductivity type formed in the third semiconductor layer, wherein the first and second wells are spaced apart, and wherein the first and second wells contact the second semiconductor layer;

first and second doped regions formed in the first well, wherein the first doped region comprises the first conductivity type and the second doped region comprises the second conductivity type, and wherein the first and second doped regions are electrically coupled; and

third and fourth doped regions formed in the second well, wherein the third doped region comprises the first conductivity type and the fourth doped region comprises the second conductivity type, and wherein the third and fourth doped regions are electrically coupled.

Claim 10 (cancelled).

11. (currently amended): The SCR device of claim 9 wherein the first semiconductor layer has a dopant concentration of about $1.0x10^{13}$ atoms/cm^3, and a thickness of about 1.5 to about 3.0 microns.

12. (previously presented): The SCR device of claim 9 further comprising a deep isolation trench extending from a surface of the third semiconductor layer into the semiconductor substrate.

13. (previously presented): The SCR device of claim 9 further comprising a deep contact trench extending from a surface of the third semiconductor layer into the semiconductor substrate.

14. (previously presented): The SCR device of claim 9 further comprising an isolation region formed on a surface of the third semiconductor layer between the first and second wells.

15. (previously presented): The SCR device of claim 9 wherein the first conductivity type comprises p-type, and wherein the second conductivity type comprises n-type.

16. (withdrawn): A method for forming a high frequency SCR device including the steps of:

providing a semiconductor substrate including a first semiconductor layer of a first conductivity type, a second semiconductor layer of a second conductivity type over the first semiconductor layer, and a third semiconductor layer over the second semiconductor layer, wherein the third semiconductor layer comprises the second conductivity type, and wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer;

forming first and second wells in the third semiconductor layer, wherein the first and second wells comprise the first conductivity type, and wherein the first and second wells are spaced apart;

forming first and second doped regions in the first well, wherein the first doped region comprises the first conductivity type, and the second doped region comprises the second conductivity type; and

forming third and fourth doped regions in the second well, wherein the third doped region comprises the first conductivity type, and wherein the fourth doped region comprises the second conductivity type.

17. (withdrawn): The method of claim 16 wherein the step of providing the semiconductor substrate includes providing a semiconductor substrate having a fourth semiconductor layer formed between the first semiconductor layer and the second semiconductor layer, wherein the fourth semiconductor layer comprises the first conductivity type, and wherein the fourth semiconductor layer has a lower dopant concentration than the first semiconductor layer.

18. (withdrawn): The method of claim 16 further comprising the steps of:

forming an isolation region on a surface of the third semiconductor region between the first and second wells;

forming a first ohmic contact coupling the first and second doped regions; and

forming a second ohmic contact coupling the third and fourth doped regions.

19. (withdrawn): The method of claim 16 further comprising the step of forming a deep isolation trench that surrounds the high frequency SCR device, and that extends from a surface of the third semiconductor layer into the first semiconductor layer.

20. (withdrawn): The method of claim 16 further comprising the step of forming a deep contact trench extending from a surface of the third semiconductor layer into the first semiconductor layer.

REMARKS

Claims 1-9 and 11-20 are in the application. Claim 10 is cancelled by this amendment. Claims 16-20 have been withdrawn in view of a restriction requirement.

By this amendment, claims 6 and 11 have been amended to correct minor typographical errors. Claim 9 has been amended to more particularly set out applicants' invention. FIG. 5 and paragraph [0036] support the changes to claim 9.

Applicants believe that this amendment places the application in better form for allowance or consideration on appeal, and respectfully request its admission.

Response to 35 U.S.C. §103 Rejections

Claims 1-4, 6-13, and 15 were rejected under 35 U.S.C. §103 as being obvious over Wang et al., USP 6,365,924 (hereinafter "Wang") in view of Mori, USP 4,246,594 (hereinafter "Mori"). This rejection is respectfully traversed in view of the amendments and remarks presented hereinafter.

Claim 1 calls for a high frequency integrated circuit structure comprising a body of semiconductor material having a plurality of isolated active regions. The body semiconductor material has a first conductivity type. Internal circuitry is formed in a first active region. A second active region comprising a buried layer of a second conductivity type is formed over the body of semiconductor material and a first semiconductor layer of the second conductivity type is formed over the buried layer. The first semiconductor layer has a lower dopant concentration than the buried layer.

A first silicon controlled rectifier device is formed in the second active region. The first silicon controlled rectifier device comprises a first well region of the first conductivity type formed in the first semiconductor layer, a first doped region of the first conductivity type formed in the first well region, the buried layer, a second well region of the first conductivity type formed in the first semiconductor layer and spaced apart from the first well region, and a second doped region of the second conductivity type formed in the second well region.

A second silicon controlled rectifier device comprises the second well region, a third doped region of the first conductivity type formed in the second well region, the buried layer, the first well region, and a fourth doped region of the second conductivity type formed in the first well region.

The first and second silicon controlled rectifier devices are coupled to the internal circuitry and form an ESD structure for protecting the internal circuitry against positive and negative ESD stresses.

Applicants respectfully submit that Wang in view of Mori fails to make claim 1 obvious for the following reasons.

1. There is no motivation to combine the Wang and Mori references.

Applicants respectfully assert that there is no motivation to combine the two references. It is well accepted that obviousness can only be established by combining the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. In re Fine, 837 F.2d 1071, 5

U.S.P.Q.2d 1596 (Fed. Cir. 1988). Specifically, the Wang reference teaches a CMOS implementation (see column 4, line 31) of a dual direction SCR device, while the Mori reference teaches a conventional bipolar implementation of a stand alone unidirectional SCR switch. Moreover, Wang does not suggest that his device is suitable for a bipolar implementation, and Mori does not suggest that his device is suitable for a CMOS implementation.

Additionally, Mori's SCR structure is not symmetrical and thus is not conducive to forming an ESD structure for protecting internal circuitry against positive and negative ESD stresses. Specifically, Mori's structure places an individual SCR in each cell, and these SCR's comprise individual and isolated PNPN devices (regions 14, 18, 20, and 22), which are not symmetrical as evident in FIG. 3a.

In response to the Examiner's statement that there is sufficient motivation to combine because "both references still teach SCR devices" is not convincing because it ignores the key differences between the references set forth above. Obvious to try is not an accepted standard.

Absent applicants' invention as a roadmap to motivate the combination, applicants respectfully submit that there is no motivation to combine the references, and the obviousness rejection should be withdrawn.

2. The combination of Wand and Mori still does not make claim 1 obvious.

Assuming arguendo that there is motivation to combine the two references, the combination of Wang and Mori still does not make claim 1 obvious for several reasons. Specifically, claim 1 calls for the first and second well regions to be of one conductivity type, and the buried layer

to be of a second conductivity type. In Mori, his buried layer is the same conductivity type as his well region 14.

Additionally, since Mori's device is unidirectional, he uses individual or separate buried layers for each device, and there is no suggestion of one buried layer being part of two devices as called for in claim 1. In fact, it is clear from Mori's FIG. 3a that his individual devices are separated by a large resistance R_s.

Furthermore, the teaching of Mori would suggest at best placing a buried layer below Wang's diffused N-Well 116, and thus, it would not even be part of the two SCR devices as called for in claim 1. It would simply lower resistance as taught in the Mori reference. Applicants further submit that this is not a minor difference because with their implementation with the buried layer being part of the SCR devices, the buried layer provides, among other things, a relatively high holding voltage, which allows applicants' structure to overcome deficiencies of prior art structure like Wang's, which have a tendency to remain in a clamped "on" state when parasitic triggering events occur (see paragraphs [0027] and [0040] in applicants' specification).

3. The combination of Wang and Mori would destroy or impair the intended function of the Wang device.

It is further accepted that a prima facie case of obviousness cannot be properly made if a proposed modification or combination would destroy or impair the function of the device disclosed in a reference. In re Gordon, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). Since Wang's structure is specifically shown as a CMOS implementation, isolation in conventional CMOS technology is achieved by the fact that the junction formed between the P-

Wang's diffused N-Well 116, and thus, Wang's two P-base regions would not contact the second semiconductor layer as called for in claim 9. Applicants further submit that this is not a minor difference because with their implementation, the second semiconductor layer provides, among other things, a relatively high holding voltage, which allows applicants' structure to overcome deficiencies of prior art structure like Wang's, which have a tendency to remain in a clamped "on" state when parasitic triggering events occur (see paragraphs [0027] and [0040] in applicants' specification).

Thus, for at least these reasons, applicants respectfully submit that claim 9 is allowable.

Claims 11 and 15 depend from claim 9 and are believed allowable for at least the same reasons as claim 9.

Claims 5 and 14 were rejected under 35 U.S.C. §103 as being obvious over Wang in view of Mori, and further in view of Duvvury et al., USP 6,365,940. This rejection is respectfully traversed.

Applicants respectfully submit that the Duvvury reference does not make up the deficiencies of Wang and Mori as discussed above.

Claim 5 depends from claim 1 and thus, is believed allowable for at least the same reasons as claim 1.

Claim 14 depends from claim 9 and thus, is believed allowable for at least the same reasons as claim 9.

Claims 8 and 12 were rejected under 35 U.S.C. §103 as being obvious over Wang in view of Mori, and in further view of Pavier et al. This rejection is respectfully traversed.

Applicants respectfully submit that the Pavier reference does not make up for the deficiencies of Wang and Mori as discussed above.

Claim 8 depends from claim 1 and further calls for a deep isolation trench formed in the body of semiconductor material for isolating the ESD structure from the internal circuitry, wherein the deep isolation trench includes a dielectric layer. Applicants respectfully submit that claim 8 is allowable for the same reasons as claim 1. Additionally, applicants respectfully submit that absent applicants' invention as a roadmap, there is simply no motivation whatsoever to combine the Pavier reference with Wang and Mori. Specifically, Pavier is not dealing with ESD issues, nor he is dealing with SCR devices. Thus, applicants submit that claim 8 is allowable for this additional reason.

Claim 12 depends from claim 9 and is believed allowable for the same reasons as claim 9. Claim 12 further calls for a deep isolation trench extending from a surface of the third semiconductor layer into the semiconductor substrate. Applicants respectfully submit that claim 12 is allowable for the same reasons as claim 9. Additionally, applicants respectfully submit that absent applicants' invention as a roadmap, there is simply no motivation whatsoever to combine the Pavier reference with Wang and Mori. Specifically, Pavier is not dealing with ESD issues, nor he is dealing with SCR devices. Thus, applicants submit that claim 12 is allowable for this additional reason.

Claim 13 was rejected under 35 U.S.C. §103 as being obvious over Wang in view of Mori, and in further view of Norstrom et al. This rejection is respectfully traversed.

Applicants respectfully submit that the Norstrom reference does not make up for the deficiencies of Wang and Mori as discussed above.

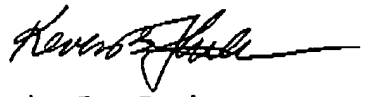
Claim 13 depends from claim 9 and further calls for a deep contact trench extending from a surface of the third semiconductor layer into the semiconductor substrate. Claim 13 is believed allowable for the same reasons as claim 9. Additionally, applicants respectfully submit that absent applicants' invention as a roadmap, there is simply no motivation whatsoever to combine the Norstrom reference with Wang and Mori. Specifically, Norstrom is not dealing with ESD issues, nor he is dealing with SCR devices. Thus, applicants submit that claim 13 is allowable for this additional reason.

In view of all of the above, it is believed that the claims are allowable, and the case is in condition for allowance, which action is earnestly solicited.

If there are any remaining issues that the Examiner believes can be resolved by telephone conference, applicants' attorney respectfully requests that the Examiner contact him at 602.244.4885.

Respectfully submitted,

Evgueniy N. Stefanov et al.



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